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| **Batch: B4 Roll No.: 16010122221 Experiment / assignment / tutorial No.: 4** |

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| **Title:** 4 bit Magnitude Comparator |

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**Objective:** Design a 2-bit comparator using logic gates and verify 4-bit magnitudecomparator using IC 7485

**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

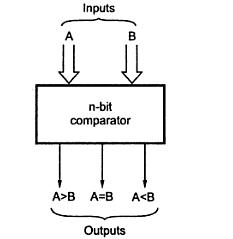
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**Books/ Journals/ Websites referred:**

* VLab Link: <http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/experimentlist.html>
* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* http://elnsite.teilam.gr/ebooks/digital\_design/lab/dataSheets\_page/7485.pdf

**Pre Lab/ Prior Concepts:**

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



**Two Bit Magnitude Comparator Implementation Details:**

**Truth Table**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A1 | A0 | B1 | B0 | A > B | A = B | A < B |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

**From the Truth Table:**

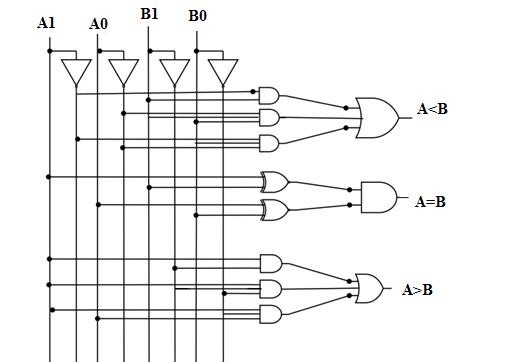
**(A<B) =** A1’B1 + A0’B1B0 + A1’A0’B0

**(A=B) =** (A1XORB1). (A0XORB0)

**(A>B) =** A1B1’ + A0B1’B0’ + A1A0B0’

# Logic Diagram of 2 bit Comparator

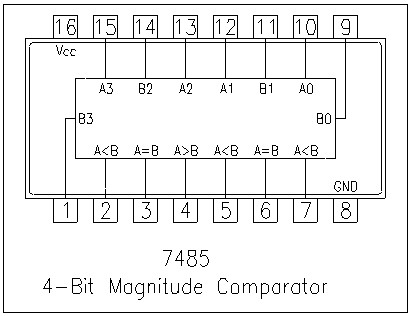
**Logic Diagram of 2 bit Comparator**



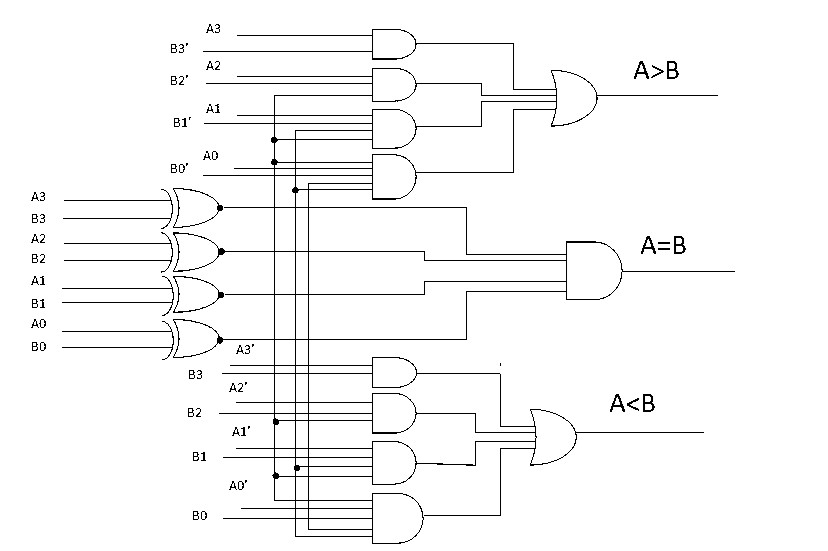
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**Four Bit Magnitude Comparator Implementation Details**

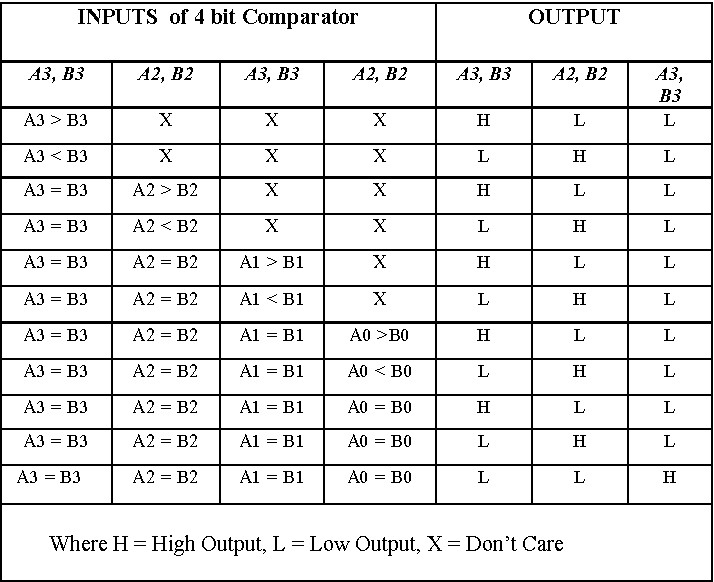
# Pin Diagram of IC 7485



# Logic Diagram of IC 7485



**Comparing Table**



\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Conclusion:**

Through this experiment we learnt the concept of comparators – 1 bit, 2 bit and 4 bits. We also learnt to implement them through logic diagrams and truth tables.

**Post Lab Descriptive Questions**

1. Design a 1- bit magnitude comparator using logic gates.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **f (A>B)** | **f (A=B)** | **f (A<B)** |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

**From the truth table:**

Equation of A > B = A.B’

Equation of A < B = A’.B

Equation of f(A = B) = A’.B’ + A.B = A XNOR B = (A.B’ + A’.B)’ = (f(A>B)+f(A<B))’

**Logic Diagram:**

